

1/00
J/06 H04L
7/04

FIG.1

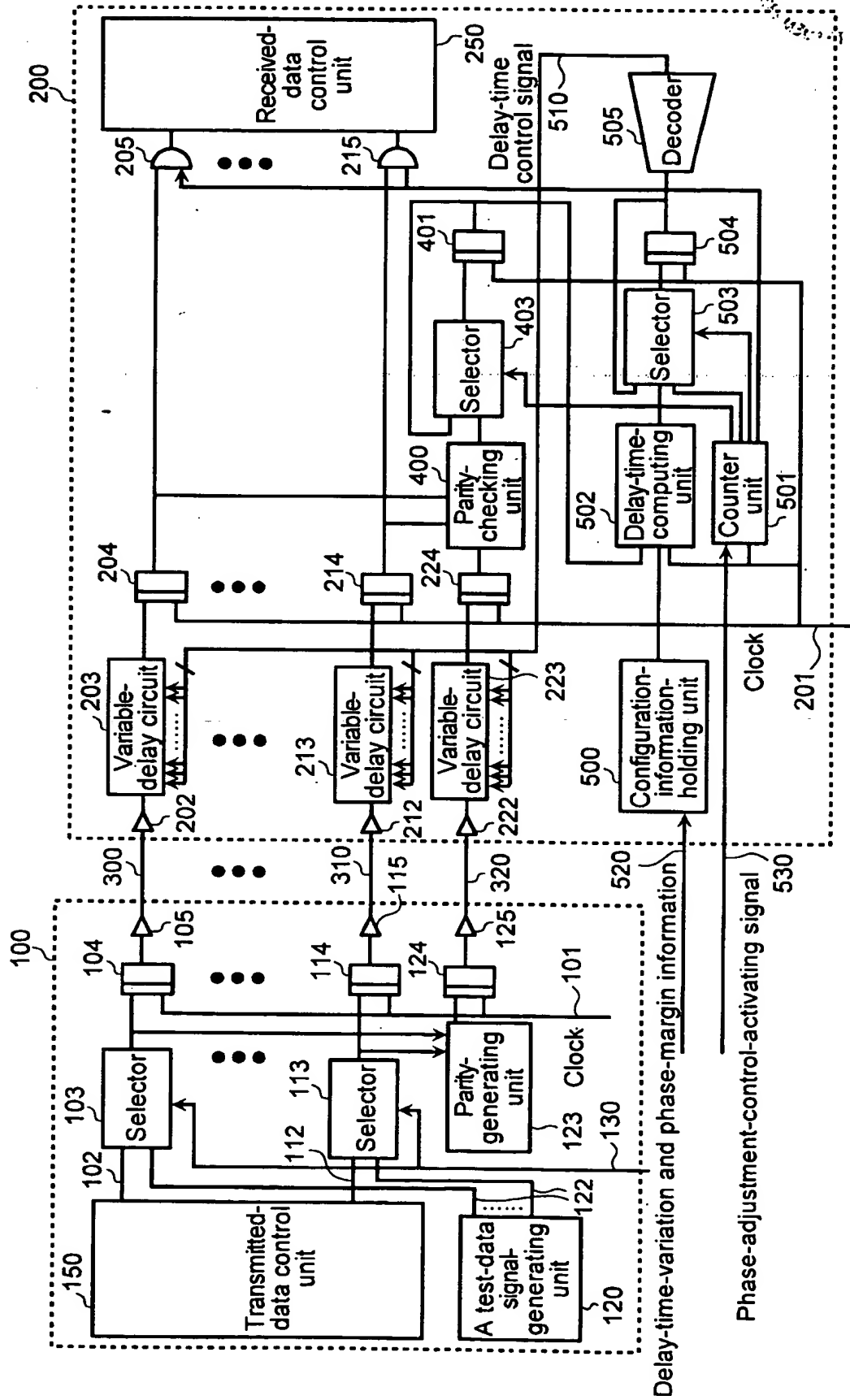


FIG.2

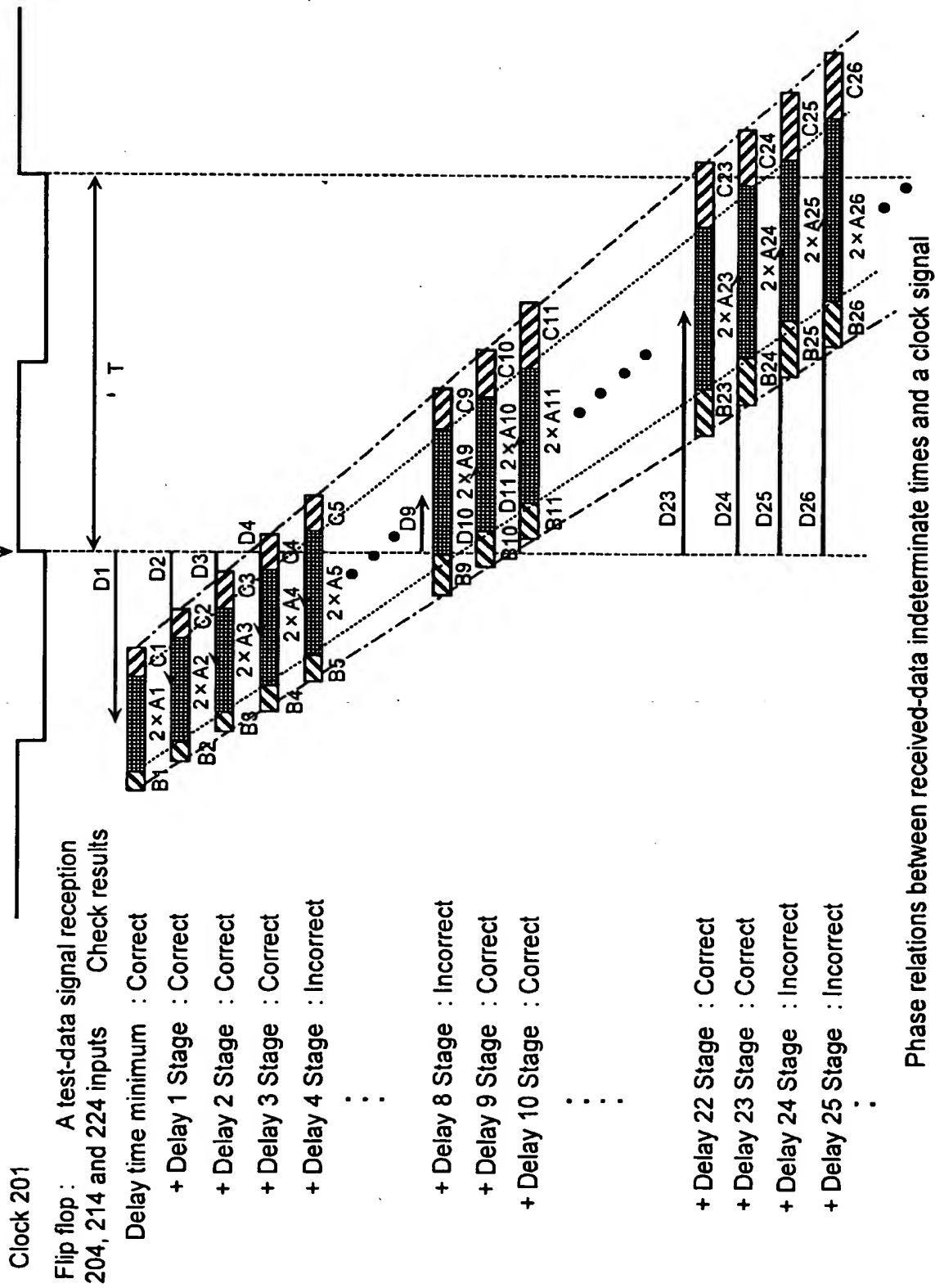


FIG.3

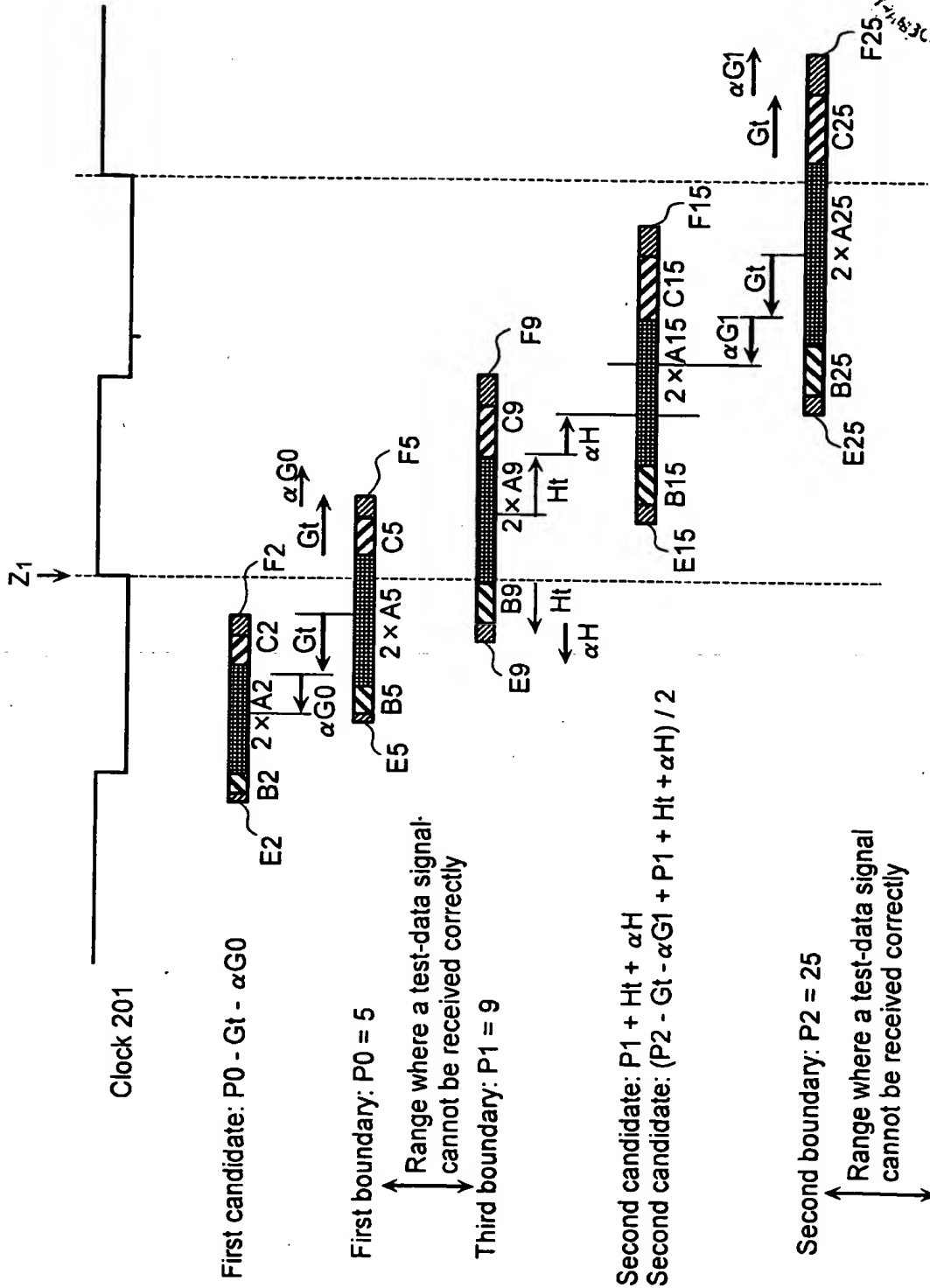
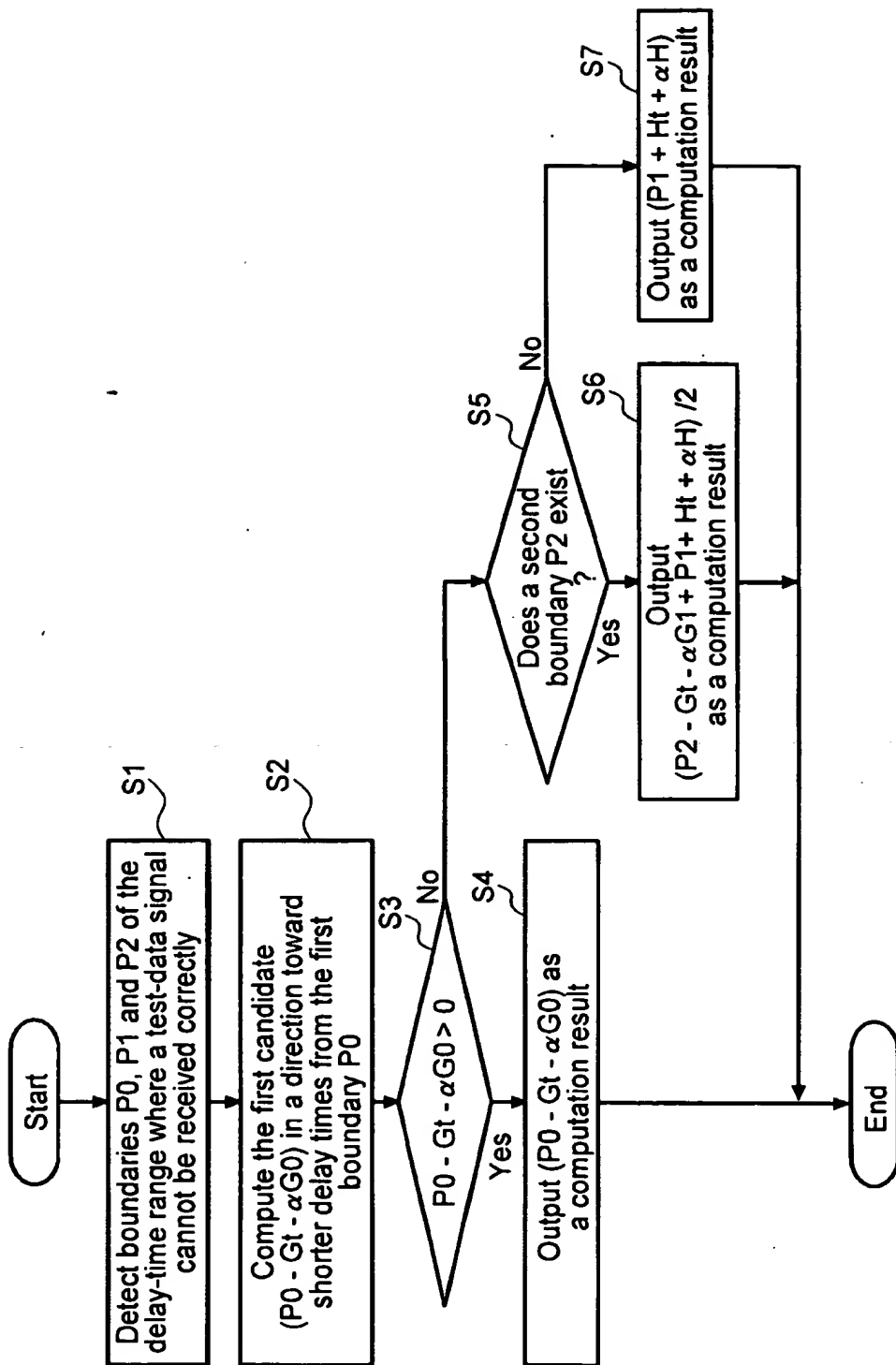


FIG.4



Algorithm of the delay-time computation

FIG. 5

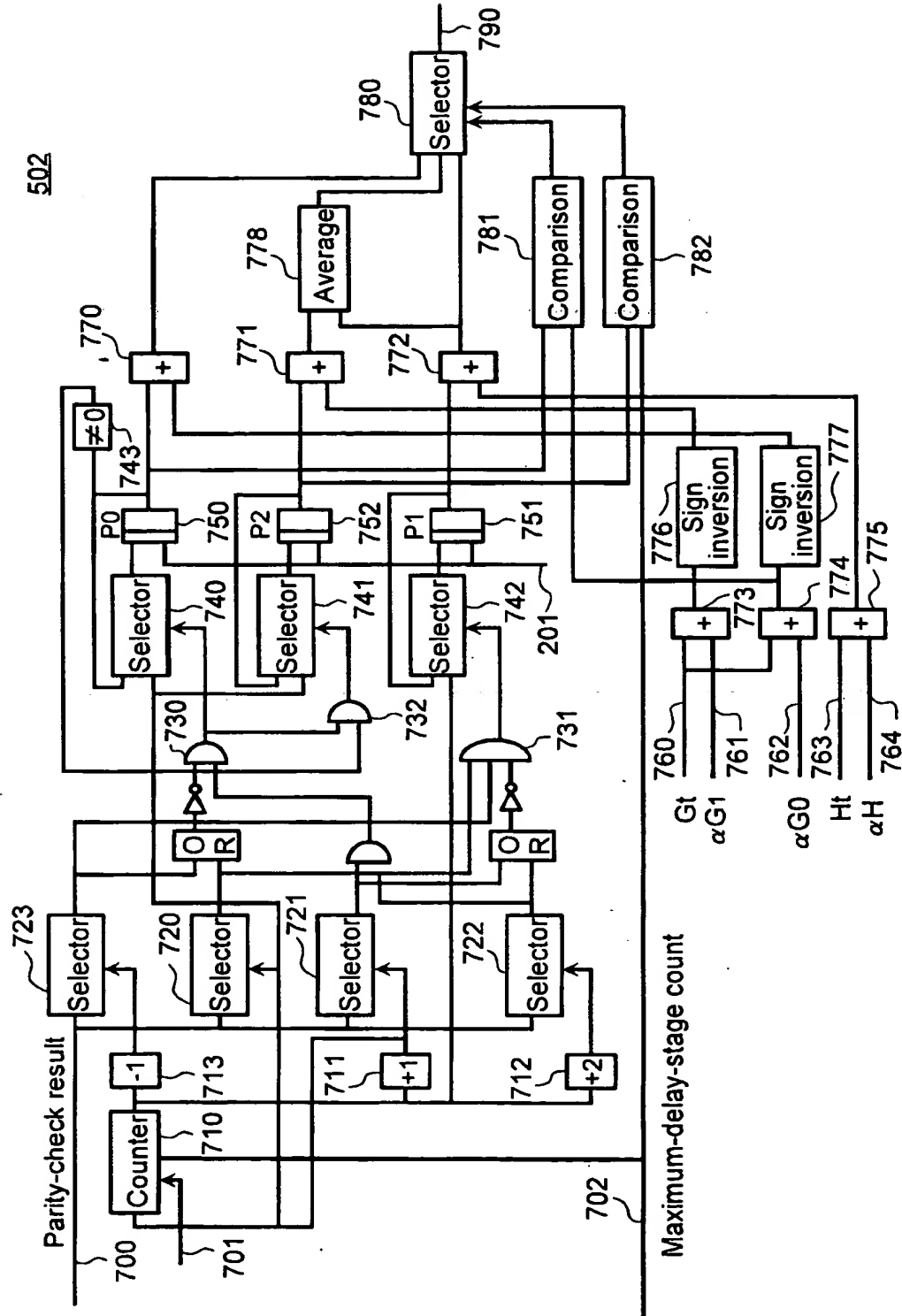
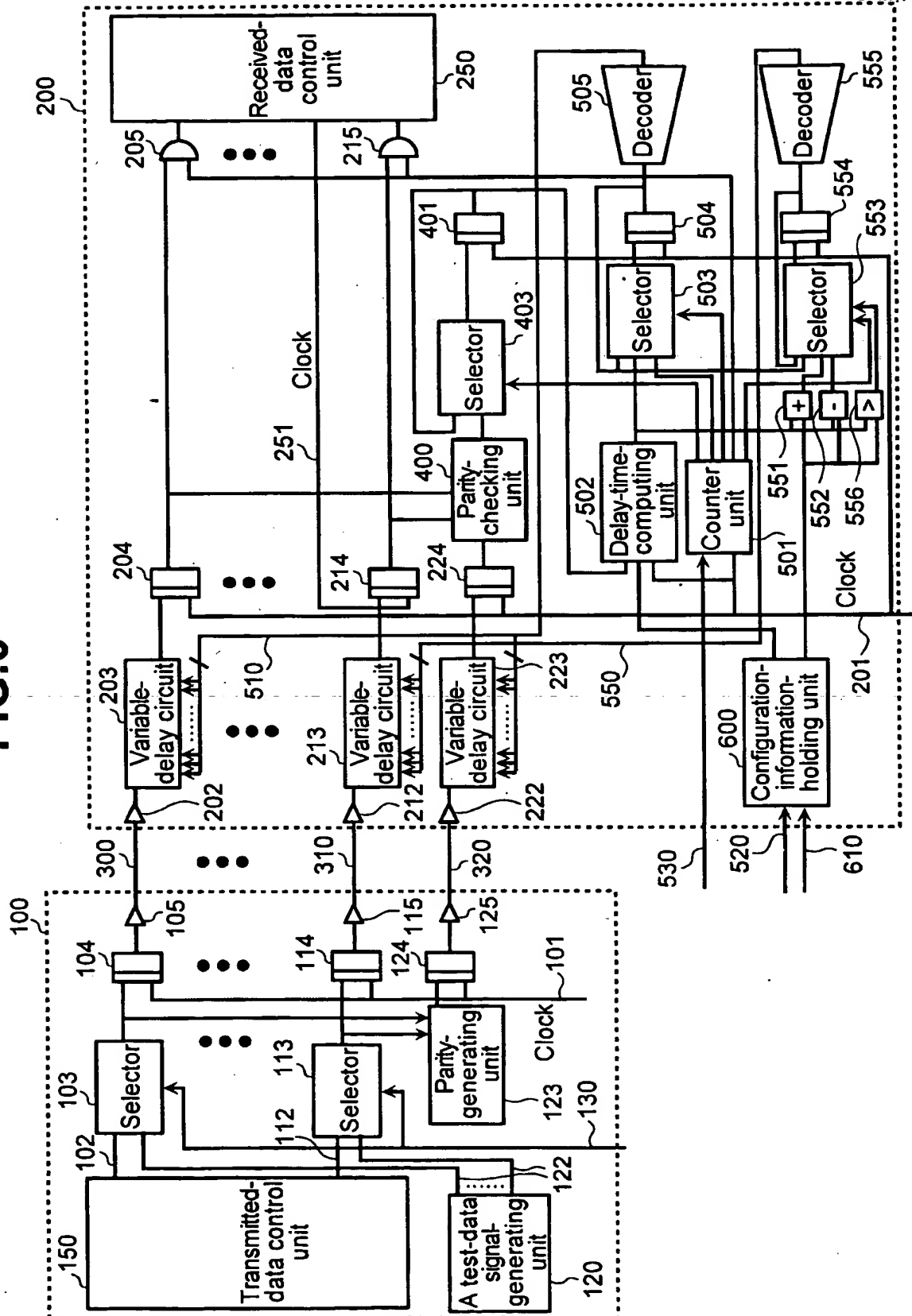


FIG. 6



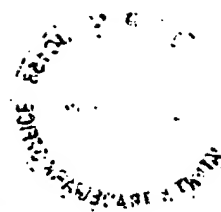


FIG.7

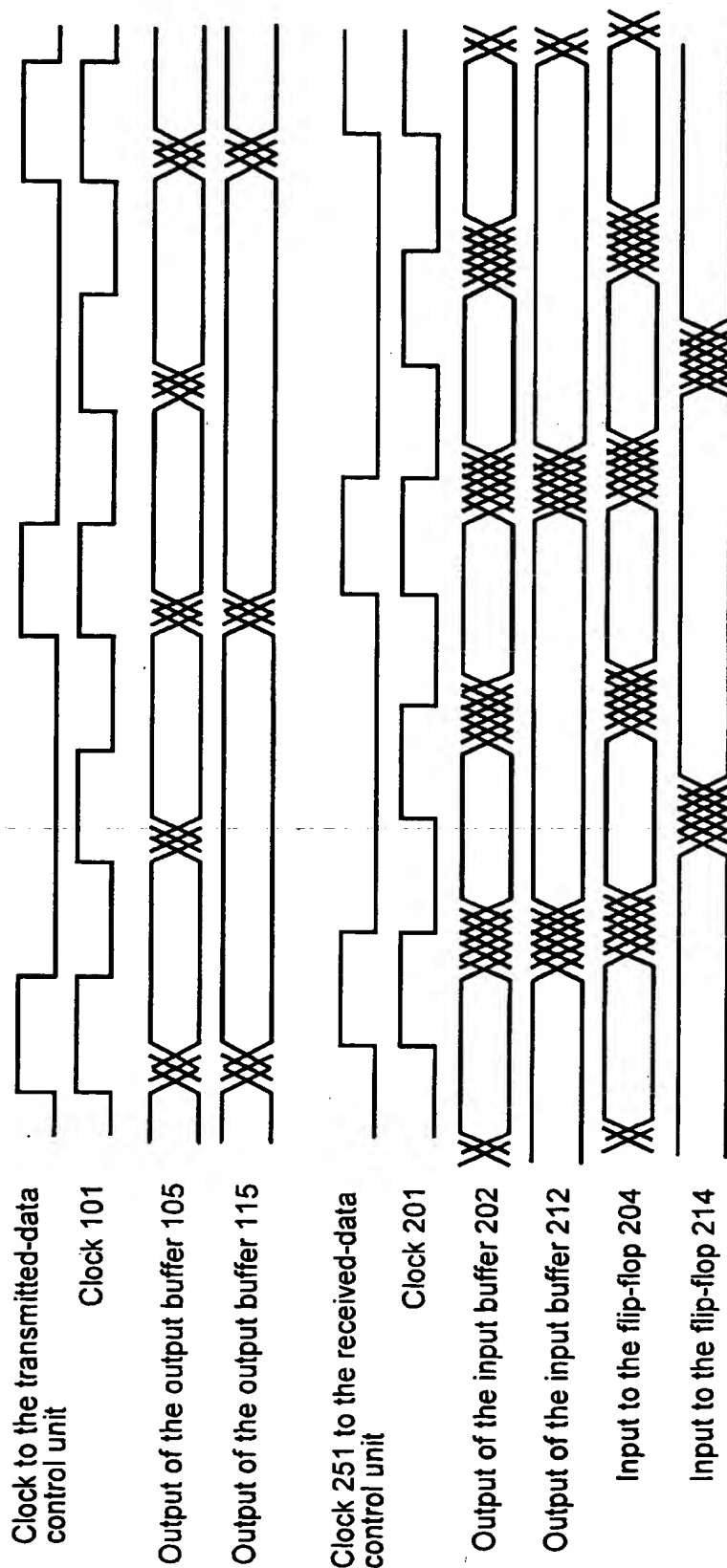


FIG. 8.

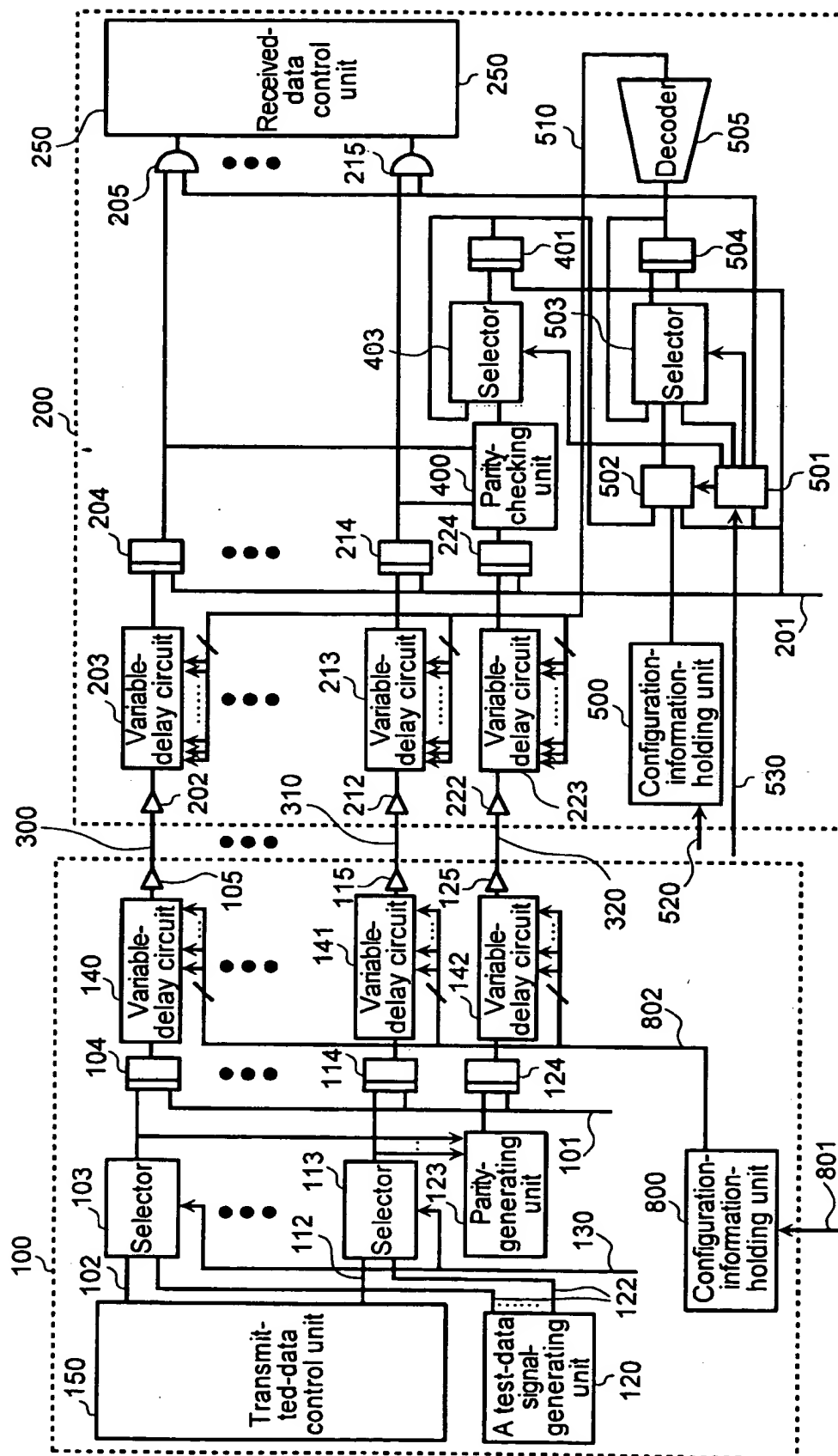
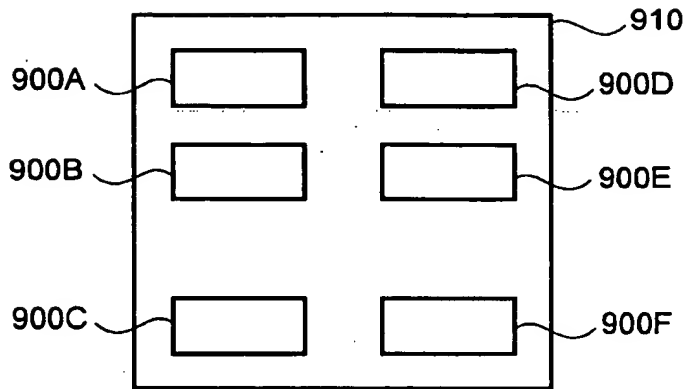


FIG.9

Single Circuit



Multi-Circuit
Chip



Multi-Chip
Device

